6. (a) Draw comparison between Write-Through Cache and Write-Back Cache. **8**

(b) Describe IEEE future bus. **7**

Unit IV

7. Describe parallel programming environment. List advantages and disadvantages of CM-5 with respect to Y-MP and Paragon. **15**

8. (a) Name and explain the techniques used for partitioning in parallel models. **8**

(b) Name and explain any *two* parallel programming models. **7**

18H1

B. Tech. EXAMINATION, 2024

(Eighth Semester)

(C-Scheme) (Main & Re-appear)

(CSE)

CSE402C

ADVANCED COMPUTER ARCHITECTURE

Time : 3 *Hours*] [*Maximum Marks :* 75

Before answering the question-paper candidates should ensure that they have been supplied to correct and complete question-paper. No complaint, in this regard, will be entertained after the examination.

Note : Attempt *Five* questions in all, selecting at least *one* question from each Unit. All questions carry equal marks.

Unit I

1. (a) A 400 MHz processor was used to execute a bench mark program with the following instruction mix and clock cycle counts :

Instruction type	Instruction count	Clock cycle count
Int Arithmetic	450000	1
Data Transfer	320000	2
Floating Point	150000	2
Control Transfer	80000	2

Define and determine the Effective CPI, MIPS rate and Execution time. **8**

(b) List and explain *five* basic scalability metrics affecting system performance. **7**

2. (a) Write the Bernstein's conditions for parallelism. **8**

(b) Taking example of 2 × 2 matrix multiplication, show the effect of fine-grain and coarse-grain programs on scheduling, making required assumptions. **7**

Unit II

3. (a) Differentiate between CISC and RISC instruction set architecture. **8**

(b) Linear pipeline and Non-Linear pipeline processors. **7**

4. (a) In instruction pipelining, how can Internal data forwarding improve throughput of pipelined processor. **8**

(b) Explain Cache coherence problem and how can we solve it. **7**

Unit III

5. Consider a cache (M1) and memory (M2) hierarchy with the following : **8+7**

M1 : 16k works, 50 ns access time, M2 : 1M words, 400 ns access time

Assume 8 word cache blocks and a set size of 256 words with set associative mapping.

(i) Draw block diagram and show the mapping between M2 and M1.

(ii) Calculate the effective memory access time with a cache hit ratio of h = 0.95.